SEMICONDUCTOR

SC0865M2

SILICON CARBIDE SCHOTTKY DIODE
Reverse Voltage - 650V
Forward Current -8A

Features

- Zero Reverse Recovery Current
- Zero Forward Recovery Voltage
- Positive Temperature Coefficient on VF
- Temperature-independent Switching
- 175℃ Operating Junction Temperature

Benefits

- Replace Bipolar with Unipolar Device
- Reduction of Heat Sink Size
- Parallel Devices Without Thermal Runaway
- Essentially No Switching Losses

Applications

- Switch Mode Power Supplies
- Power Factor Correction
- Motor drive, PV Inverter, Wind Power Station

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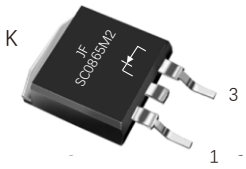

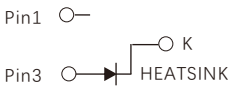

V_{RRM}	=	650	V
I_F ($T_C \leq 135℃$)	=	11	A
Q_C	=	22	nC

Maximum Ratings

Symbol	Parameter	Value	Unit	Test Conditions	Note
V_{RRM}	Repetitive Peak Reverse Voltage	650	V	T_J = 25℃	
V_{RSM}	Surge Peak Reverse Voltage	650	V	T_J = 25℃	
V_R	DC Blocking Voltage	650	V	T_J = 25℃	
I_F	Forward Current	24 11 8	A	$T_C \leqslant$ 25℃ $T_C \leqslant$ 135℃ $T_C \leqslant$153℃	
I_{FSM}	Non-Repetitive Forward Surge Current	50	A	T_J = 25℃, t_p = 8.3ms, Half Sine Wave	
P_{tot}	Power Dissipation	107	W	T_J = 25℃	Fig. 3
T_J, T_{STG}	Operating Junction and Storage Temperature	-55 to 175	℃		

Electrical Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_F	Forward Voltage	1.4 1.7	1.65 2.3	V	I_F = 8A, T_J = 25℃ I_F = 8A, T_J = 175℃	Fig. 1
I_R	Reverse Current	1 5	20 100	μA	V_R = 650V, T_J = 25℃ V_R = 650V, T_J = 175℃	Fig. 2
C	Total Capacitance	520 50 41	/	pF	V_R = 0V, T_J = 25℃, f = 1MHz V_R = 200V, T_J = 25℃, f = 1MHz V_R = 400V, T_J = 25℃, f = 1MHz	Fig. 5
Q_C	Total Capacitive Charge	22	/	nC	V_R = 650V, I_F = 8A di/dt = 200A/μs, T_J = 25℃	Fig. 4

Thermal Characteristics

Symbol	Parameter	Typ.	Unit	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	1.4	℃/W	Fig. 6
$R_{\theta JA}$	Thermal Resistance from Junction to Ambient	80	℃/W	
T_{sold}	Soldering Temperature	260	℃	

Typical Performance

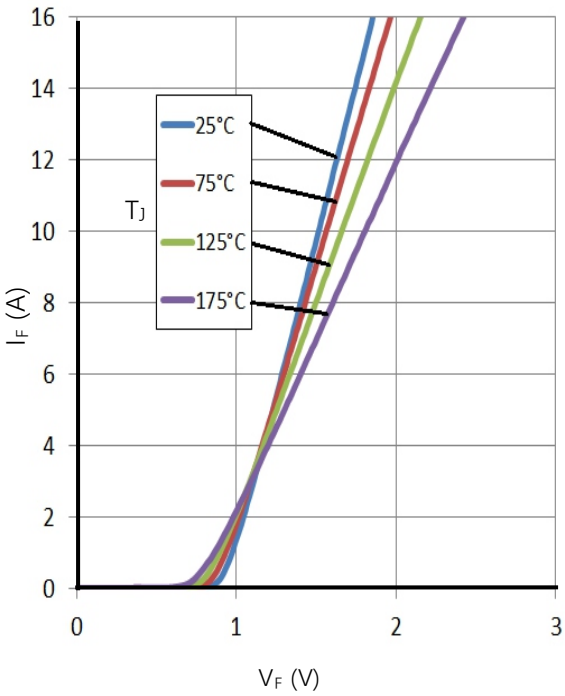

Figure 1. Forward Characteristics

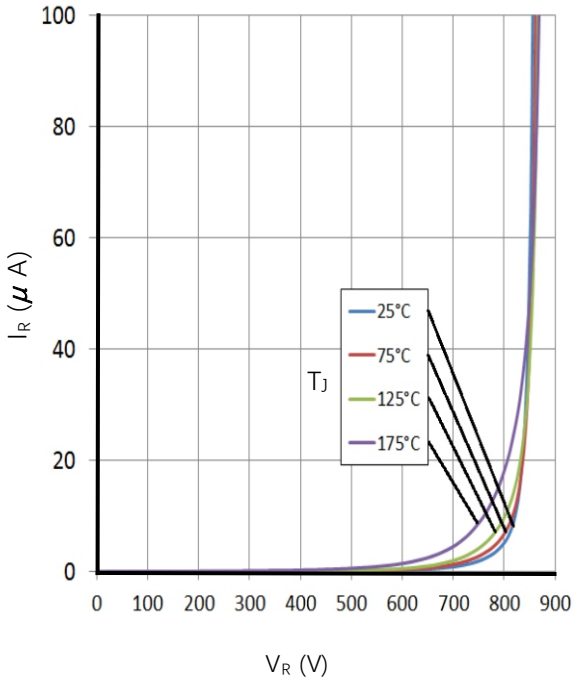

Figure 2. Reverse Characteristics

Typical Performance

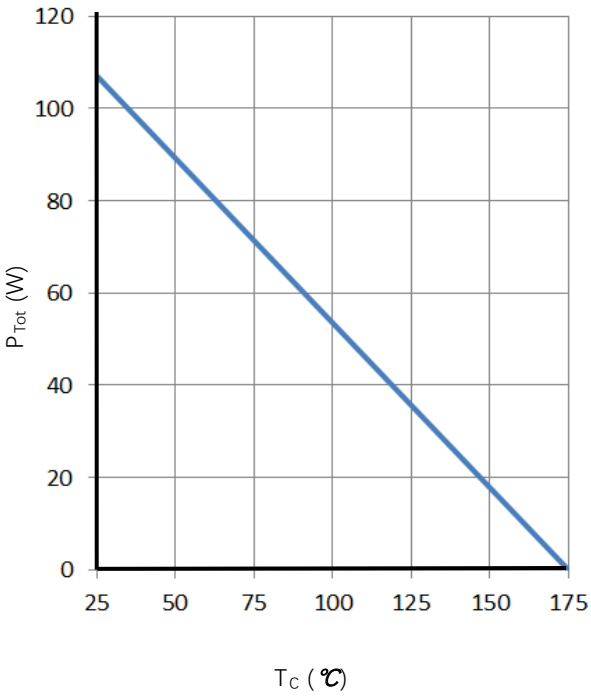

Figure 3. Power Derating

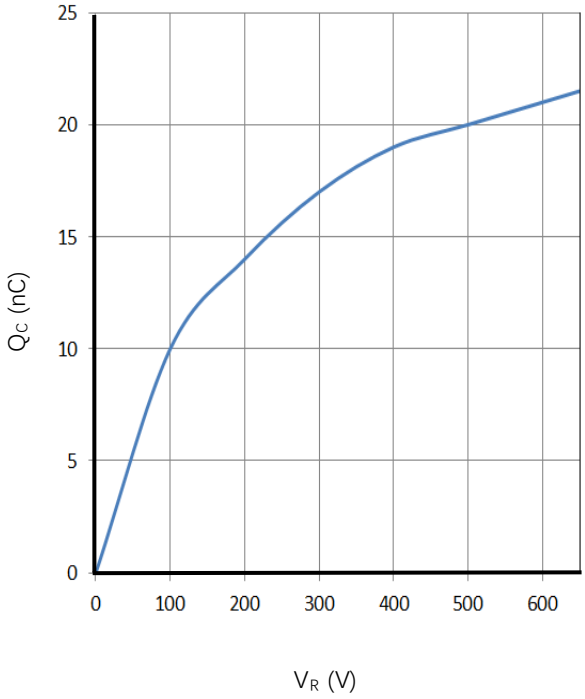

Figure 4. Total Capacitive Charge vs. Reverse Voltage

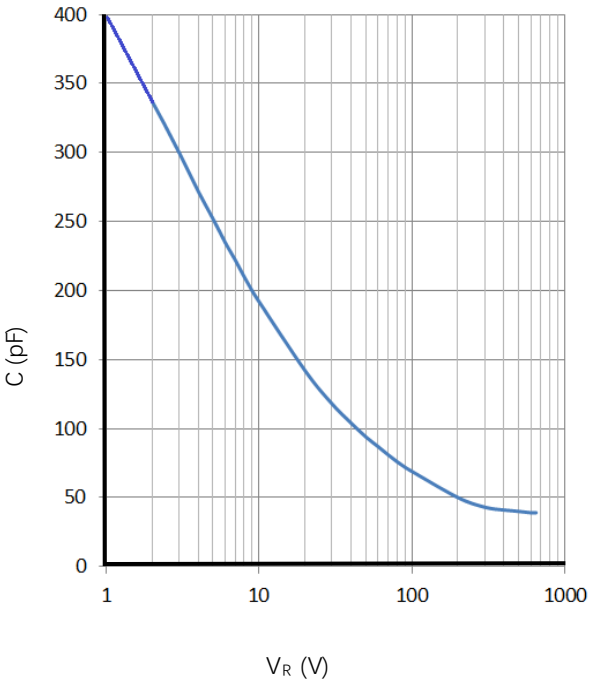

Figure 5. Total Capacitance vs. Reverse Voltage

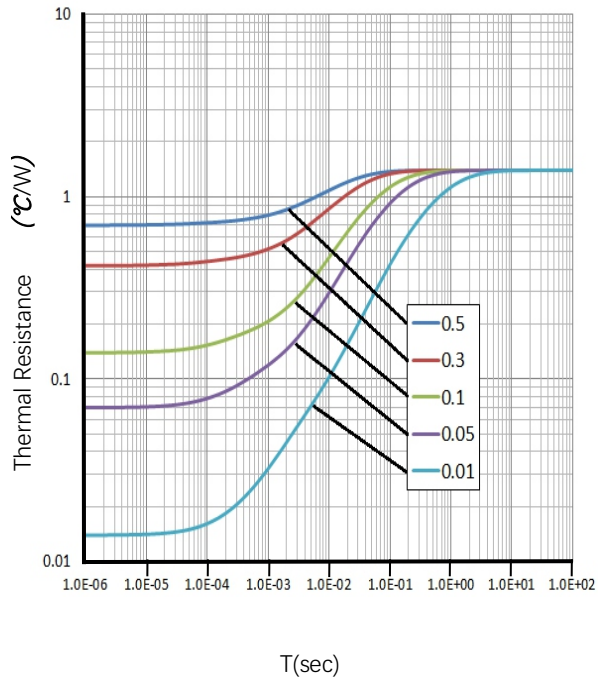

Figure 6. Transient Thermal Impedance

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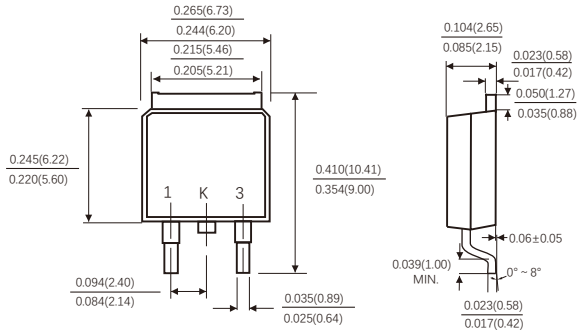

Suggested Pad Layout

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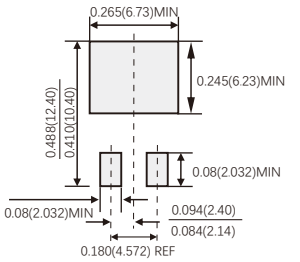

(设计者可参考推荐值根据焊接工艺
要求自行确定适合的焊盘尺寸)
(Designers can refer to the recommended
values according to the manufacturing process
requirements to determine the appropriate pad size)

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